In the claims:

Claim 1 (currently amended) A field effect transistor comprising:

a region of semiconductor material doped a first conductivity type;

spaced apart source/drain ~~and drain regions~~ pockets of ~~opposite~~ said first conductivity type, ~~both~~ said source/drain pockets ~~region and said drain region~~ disposed in said region of semiconductor material and ~~a~~ counterdoped regions of ~~first~~ opposite conductivity type disposed within said source/drain regions forming ~~a~~ source/drains ~~and within said drain region forming a drain and isolated from the remaining portion of said region of semiconductor material by said source region and said drain region~~;

a ~~counterdoped~~ channel region disposed in said region of semiconductor material between said source/drain regions ~~and said drain region;~~, said ~~counterdoped~~ channel region having a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region being the primary conduction channel of said transistor and having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source and said drain.

Claim 2 (canceled)

Claim 3 (previously amended) The field effect transistor of Claim 1, wherein the dopant comprises an n-type dopant.

Claim 4 (original) The field effect transistor of Claim 1, wherein the first doped region comprises a first dopant, and wherein the second doped region comprises a second dopant different from the first dopant.

Claim 5 (original) The field effect transistor of Claim 4, wherein the first dopant comprises arsenic, and wherein the second dopant comprises phosphorus.

Claim 6 (original) The field effect transistor of Claim 1, further comprising a first pocket surrounding the source, and a second pocket surround the drain, the first and second pockets each having a higher dopant concentration than the source and drain regions.

Claim 7 (currently amended) A semiconductor device comprising:

a substrate of a first conductivity type containing a plurality of field effect transistors, at least one of the field effect transistors having a ~~counterdoped~~ channel of opposite conductivity type, a source region of said first conductivity type adjacent to the channel, a drain region of said first conductivity type adjacent to the channel and spaced from said source, all disposed in said substrate, and a gate overlying the channel;

said ~~counterdoped~~ channel comprising a first region of one of undoped or counterdoped opposite conductivity type and a second doped region underlying the first region ~~of~~ counterdoped said opposite conductivity type, said second counterdoped region having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source region and said drain region.

Claim 8 (original) The semiconductor device of Claim 7, wherein the channel of the field effect transistor further comprises a surface doped layer overlying the subsurface doped layer.

Claim 9 (original) The semiconductor device of Claim 8, wherein the surface doped layer comprises a first concentration of a dopant, and wherein the subsurface doped layer comprises a second concentration of the dopant, the first concentration being greater than the second concentration.

Claim 10 (original) The semiconductor device of Claim 9, wherein the dopant comprises an n-type dopant.

Claim 11 (original) The semiconductor device of Claim 8, wherein the surface doped layer comprises a first dopant, and wherein the subsurface doped layer comprises a second dopant different from the first dopant.

Claim 12 (original) The semiconductor device of Claim 11, wherein the first dopant comprises arsenic, and wherein the second dopant comprises phosphorus.

Claim 13 (original) The semiconductor device of Claim 7, further comprising a first doped pocket surrounding the source and a second doped pocket surrounding the drain, the first and second pockets each having a higher dopant concentration than the source and drain regions.

Claim 14 (currently amended) A method for forming a field effect transistor, comprising the steps of:

providing a region of semiconductor material doped a first conductivity type;

forming a source region of said first conductivity type and a drain region of said first conductivity type, both said source region and said drain region disposed in said region of semiconductor material and separated by a ~~counterdoped~~ channel region disposed in said region of semiconductor material;

forming said ~~counterdoped~~ channel region by forming a first region in said channel region of one of undoped or opposite conductivity counterdoped type; and

doping said channel region with a ~~second~~ dopant to form a second counterdoped region underlying the first region of said opposite conductivity type, said second doped region having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source region and said drain region.